Efficient Fault Ride-Through Scheme for Three Phase Voltage Source Inverter-Interfaced Distributed Generation Using DC Link Adjustable Resistive type Fault Current Limiter

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***Abstract*—This paper proposes a DC link adjustable resistive type fault current limiter (AR-FCL) based-voltage source inverter (VSI) fault ride-through (FRT) capability improvement, which is new approach of using FCLs. Instead of using three phase FCLs in AC side of the VSI, just one single phase proposed AR-FCL is connected in series with DC side of the VSI. During normal operation, the AR-FCL does not have effect on the VSI performance. When fault happens, the AR-FCL limits AC side fault currents in faulty phases to safe area operation of semiconductor devices of inverter, and does not affect healthy lines. The desired limited fault current value can be achieved by discharging and charging of DC inductor using large resistance, which enters and retreats by turning off and on of the AR-FCL's semiconductor switch, respectively. The VSI does not require to change its control strategy from normal to fault mode operation. Consequently, wind-up and latch-up problems are smoothed. Analytical analysis is provided in each switching interval to highlight effectiveness of the AR-FCL on the VSI fault current limitation. The proposed FRT scheme is validated through both extensive simulation studies in PSCAD/EMTDC environment and three-phase experimental prototype for all symmetrical, asymmetrical, and transient faults.**

Keywords— **Voltage-sourced inverter (VSI); symmetrical and asymmetrical grid faults; fault ride-through (FRT); adjustable resistive type fault current limiter (AR-FCL).**

I. INTRODUCTION

Increased power demand and the depletion of energy resources have resulted in more attention being paid to renewable energy [1]-[3]. Over the years, power electronic converters have found wide application in numerous grid interfaced systems including distributed power generations like fuel cell [4], solar energy [5], adjustable speed drives [6] and active power filters [7]. Most of these systems employ three phase voltage source inverter (VSI) whose functionality is to exchange variable power with the utility grid.

The VSIs employ semiconductor devices (SDs) with limited over current withstand capability that usually is within the range of 1-2 times of nominal current [8]. The VSI is inherently very sensitive to the grid faults. Thus, the fault condition can either trip

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out the VSI or damage its SDs [9]-[10].

Two main control strategies are proposed in the literature to control the VSIs: current control strategy (CCS) and voltage control strategy (VCS) [11]-[13]. The advantage of the CCS is that the output current of VSI can be effectively restricted to an acceptable level during the fault condition; consequently, the inverter can ride-through networks faults. However, the CCS has several drawbacks like reduction of main controller robustness and need to both voltage and current sensors. On the other hand, while the VCS has good performance during the normal operation, but high level of fault current is its main drawback [13]. By increasing the penetration level (PL) and island operation of distributed generations (DGs) in the power systems, using the VCS to control the VSIs is more acceptable than the CCS [14]. Furthermore, at high PL of the VSIs in the power system, their disconnection form the utility during the faults is not acceptable. In addition, according to [15], the impact of VSIs on the network operation with 40% PL is not negligible.

Despite the IEEE standard 1547, which recommends that the DGs should be disconnected from the network when the fault occurs in the utility grid [16], in some new grid codes, the DGs are forced to stay connected to the grid and ride-through the network faults [17]-[18]. Regarding above mentioned discussions, different studies are conducted on current limitation strategies of the VSIs during the network faults.

Reference [7] has presented simulation and experimental results of a varistor based-short circuit fault protection scheme for series active power filters. The number of elements in the mentioned protection method like series current transformers and the semiconductor switches increase the cost. Also, the VSI is disconnected after a few cycles the fault happened, which does not comply the new grid codes [18]. Some control approaches for inverter-interfaced distributed energy resources are proposed in [19] and [20] to limit inverter fault current and improve their fault ride-through (FRT) capability. However, these methods cannot be suitable for long lasting zero grid voltage. In [21], an inverter fault current limitation strategy has been introduced in a micro-grid at high PL of the VSIs. However, in [21], simulation and experimental results have not been presented to approve its proposed technique. In [22] and [23], the authors investigated fault response of the VSIs against various network faults and presented analytical and experimental results. An active and reactive power control strategy has been proposed in [24], for DG inverters, to improve their FRT capability and enable them to support grid voltage during unbalanced faults. However, operation of the proposed method has not been analyzed during transient gird faults. In [25], a control strategy has been proposed to enhance the voltage support as an ancillary service of the VSIs to meet the grid codes requirements, which needs complicated control system. A fault protection scheme against the short-circuit fault on the load side for the high-power three-phase inverters has been studied in [26] to provide high reliability for sensitive loads during transient faults. In the mentioned study, not only the malfunction of the inverter has not been considered but also it is required to change the strategy of the VSI from the VCS to the

CCS. In [27], the authors introduced a control scheme to suppress the peak of three-phase PV inverters current during asymmetrical faults. The drawback of the mentioned work is to reduce peak of current by injection current harmonics, which are not suitable during the normal operation of the power system.

An effective method to control the fault current level is to use fault current limiters (FCLs). Several types of FCLs have been studied to improve the power system performance in [28]-[31]. As it is clear, all research on the FCLs requires a three phase or three single phase sets in the AC side, which increases the FCLs' cost. Furthermore, three phase structures may affect the healthy lines during the asymmetrical grid faults. From control system point of view, each three same sets of the single phase FCLs, located in series with individual phases of the grid, needs its own control circuit, which complicates the circuit operation and requires more measurements.

This paper proposes a novel approach of using FCLs. A single phase set-up of DC link adjustable resistive type FCL (AR-FCL) is studied to enhance the FRT capability of the VSIs during symmetrical, asymmetrical, and transient grid faults. Instead of using three phase configuration of the FCLs in the AC side, just one single phase set-up of the proposed AR-FCL is connected in series with the DC side of the inverter. In the normal operation of utility grid, the AR-FCL does not have effect on the VSI system performance. During various grid faults, the fault current is restricted by discharging and charging of DC inductor using a large resistance. By turning off and on of the AR-FCL's semiconductor switch, the large resistance enters and retreats the DC side of the inverter, respectively. As a result, the inverter's output fault current is restricted to the safe operating area of the SDs. Furthermore, the proposed structure does not affect the healthy line currents during asymmetrical grid faults. The control circuit of the AR-FCL is simple and only the DC inductor current is measured and compared to the maximum permissible current of the SDs of inverter. In this way, the VSI can stay connected to the utility during the fault even at zero grid voltage as recommended by "*E.ON*" grid code [18]. Instead of using superconducting inductor in the AR-FCL, the small non-superconducting inductor is employed, which decreases initial and maintenance costs of the AR-FCL and also the cooling system with relatively large volume is removed [32]. Besides, according to [33], the problems of latch-up and wind-up arise when the inverter control strategy changes from the normal to the fault mode operation, during the fault condition. However, in the proposed scheme, the VSI operates as the VCS in the normal condition as well as in the fault condition.

II. Proposed Fault Ride Through Scheme

Fig. 1 shows configuration of the proposed FRT scheme of the VSI system. The model of the VSI for the purpose of the fault analysis can be made up under an assumption that the DC input voltage of the inverter is essentially fixed in the time frame 0-1.0 s [34]. This voltage is shown with V_{DC} in Fig. 1. To improve the FRT capability of the VSI, application of the AR-FCL is

proposed. The AR-FCL includes diode rectifier bridge, D_1 to D_4 diodes, a non-superconducting inductor (copper coil) that is modeled by a resistor r_d and an inductor L_d and finally a parallel connection of fully controllable semiconductor switch (SS) and a resistor (R) that are connected in series with the DC-inductor. A two-level VSI is used to convert DC power provided by the primary DC energy source such as DGs to AC electrical power, which is compatible with the utility. The AR-FCL is connected in series with V_{DC} as shown in Fig. 1. Also, equivalent impedance between high voltage side of the grid-connected transformer and inverter output terminals are modeled by $Z_{eq}=r_s+j\omega L_s$ in Fig. 1. The utility is modeled by an infinite bus AC system; thus, it is an ideal sinusoidal three-phase voltage source with a constant frequency and voltage (V_{an}, V_{bn} and V_{cn} in Fig. 1), where ω and V_ϕ stand for its angular frequency and effective voltage value in each phase, respectively. In common current limiting strategies, to limit the fault current, the FCLs should be connected in series with the individual phases in the AC side of the VSI. This approach is the well-known application of the FCLs in the power system as discussed in [28]-[30]. But in the proposed scheme, just one single set of the AR-FCL, which is placed in the DC side of the VSI, is employed to limit the VSI's fault current in all three phases during all types of the grid fault. So, the proposed structure results in considerable reduction in the current limiting costs of the FCLs. Also, from the power circuit topology point of view, the AR-FCL uses the diode rectifier bridge and the fully controllable SS as a high speed switch.

III. Principle of Operation of the AR-FCL

In the normal operation of the power system, the SS is close and bypasses the R. By selecting the proper value for L_d, it is possible to achieve a nearly DC current through the DC inductor. However, it is evident that increasing the L_d decreases the ripple of DC inductor current i_d. This leads to short circuit of L_d during the steady state operation. If the voltage drops on the diodes of single phase rectifier, the SS, and the small DC inductor resistances are neglected, the AR-FCL does not affect the normal

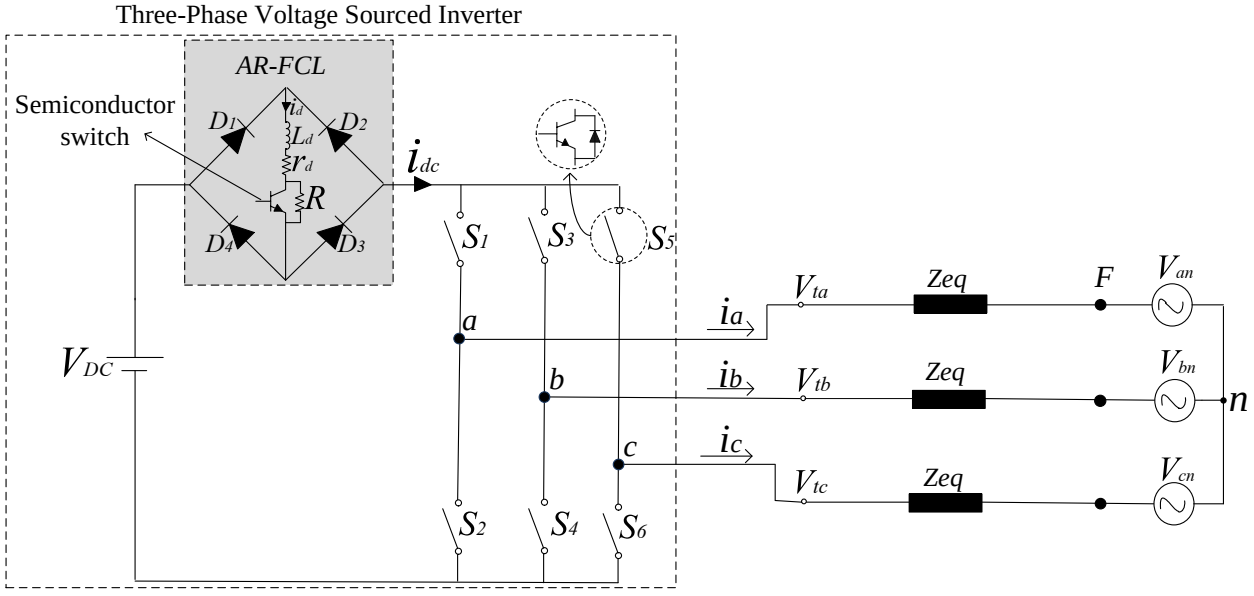

Fig. 1. Power circuit topology of the proposed fault ride-through configuration for the VSI.

operation of the VSI. When fault occurs in the power system in either one phase or some phases, the DC inductor of the AR-FCL prevents severe *di/dt* at the first moments of the fault and its current increases almost linearly. If the fault lasts for a long time, the current through the DC inductor will continue to increase. As soon as the current through the DC inductor reaches to a pre-defined value, the control circuit operates and turns off the SS. So, the *R* is connected in series with the DC inductor. Therefore, the absorbed energy of the AR-FCL's inductor discharges and the current of the DC inductor decreases. It is evident that, as the DC inductor current lies blew the pre-defined value, the control circuit operates and turns on the SS. In this way, the DC inductor current as well as the inverter output AC currents are restrained to the pre-defined value during the fault. So, the VSI can stay connected with the utility grid during the fault condition.

Fig. 2 shows the control circuit of the AR-FCL. In this study, the DC inductor current is utilised as the control signal to turn on and turn off the SS. This control system does not need any parameters to measure in the AC side of the VSI. Therefore, when the DC inductor current lies above the pre-defined value I_c, that is higher than steady state current through the DC inductor, the control circuit turns on the SS. The value of I_c should be determined based on the SDs current rating.

IV. Analytical Analysis of the Proposed Scheme

In order to analysis the operation of the VSI with the proposed AR-FCL, it is assumed that the inverter AC line currents (i_a, i_b and i_c) are pure sinusoidal. Also, the inverter is controlled by the VCS and the inverter switching signals are generated by the sinusoidal PWM (SPWM) strategy. It should be noted that, in the analytical analysis conducted in the following subsections, each semiconductor device (switches and diodes) of the inverter and the diodes of the AR-FCL are modeled by a series connection of their voltage drop, V_d, and resistance, r_{on}, in ON state. Furthermore, the SS of the AR-FCL is represented by voltage drop of V_{ss}, and resistance of r_{on}, during conducting state.

The DC link current i_{dc} can be expressed in the basis of AC line currents and switching states as follows [35]-[36]:

$$i_{dc} = S_a i_a + S_b i_b + S_c i_c \tag{1}$$

where S_a, S_b and S_c are the switching states of the phases *a*, *b* and *c*, respectively.

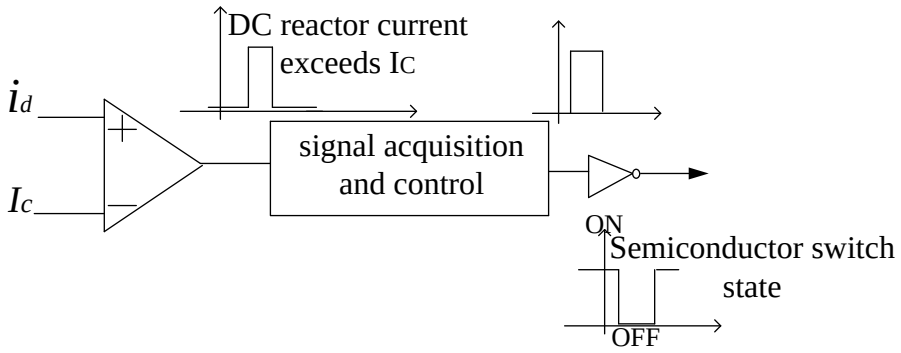

Fig. 2. Control circuit of the proposed AR-FCL.

Since, in the SPWM inverters, carrier frequency is very high compared to the fundamental output frequency, it is assumed that the value of modulating signal over one carrier period is almost constant [11], [35]. Thus, in this section, the performance of the proposed approach is explained during one carrier period [37]. For evaluation of the effectiveness of the proposed FRT scheme, a three phase short-circuit fault with fault impedance of $Z_f = r_f + jL_f\omega$ is applied at point F, as shown in Fig. 1. After fault occurrence, the circuit has two modes of operation as follows:

Mode 1: DC inductor current has not reached to I_c;

Mode 2: DC inductor current has reached to I_c.

A. *Mode 1*

Fig. 3 shows the DC link current i_{dc}, the DC inductor current i_d and the switching sequence of the interface-inverter during the fault. As evident, with changing the switching state of the SDs, i_{dc} instantaneously changes. During time interval of t_0 to t_1, switching state is (000). Fig. 4(a) shows the equivalent circuit during time interval of T_0. According to Fig. 3, from t_0 to t_1, the DC link current is less than the DC inductor current. In this condition, all diodes of the AR-FCL are ON due to the charged current in the DC inductor. In fact, the DC inductor current freewheels through the way of D_1-D_3, D_2-D_4 and SS. So the AR-FCL operates as a short circuit and it does not have effect on the inverter operation. By considering the equivalent circuit of Fig. 4(a), the DC inductor current can be written in discharging mode as follows:

$$\left(r_d + 3r_{on}\right) i_d(t) + L_d \frac{di_d(t)}{dt} = -(V_{ss} + 2V_d) \tag{2}$$

$$i_d(t) = e^{-(t-t_0)(r_d+3r_{on})/L_d} \left\{ i_1 + \frac{V_{ss} + 2V_d}{r_d + 3r_{on}} \right\} - \frac{V_{ss} + 2V_d}{r_d + 3r_{on}} \tag{3}$$

where $i_1 = i_d(t_0)$.

At $t = t_1$, the switching state changes to (100). Equivalent circuit during the time interval of t_1 to t_2 is shown in Fig. 4(b). As the equivalent circuit shows during time interval of T_1, diodes D_1 and D_3 are ON and the DC inductor current is equal with the DC link current. So, the differential equation of the DC inductor current can be expressed as follows:

$$\left(\frac{3}{2}L_e + L_d\right) \frac{di_a(t)}{dt} + \left(r_d + \frac{3}{2}r_e + \frac{9}{2}r_{on}\right) i_a(t) = V_{DC} - V_{ss} - 4V_d \tag{4}$$

Solution (4) leads to (5).

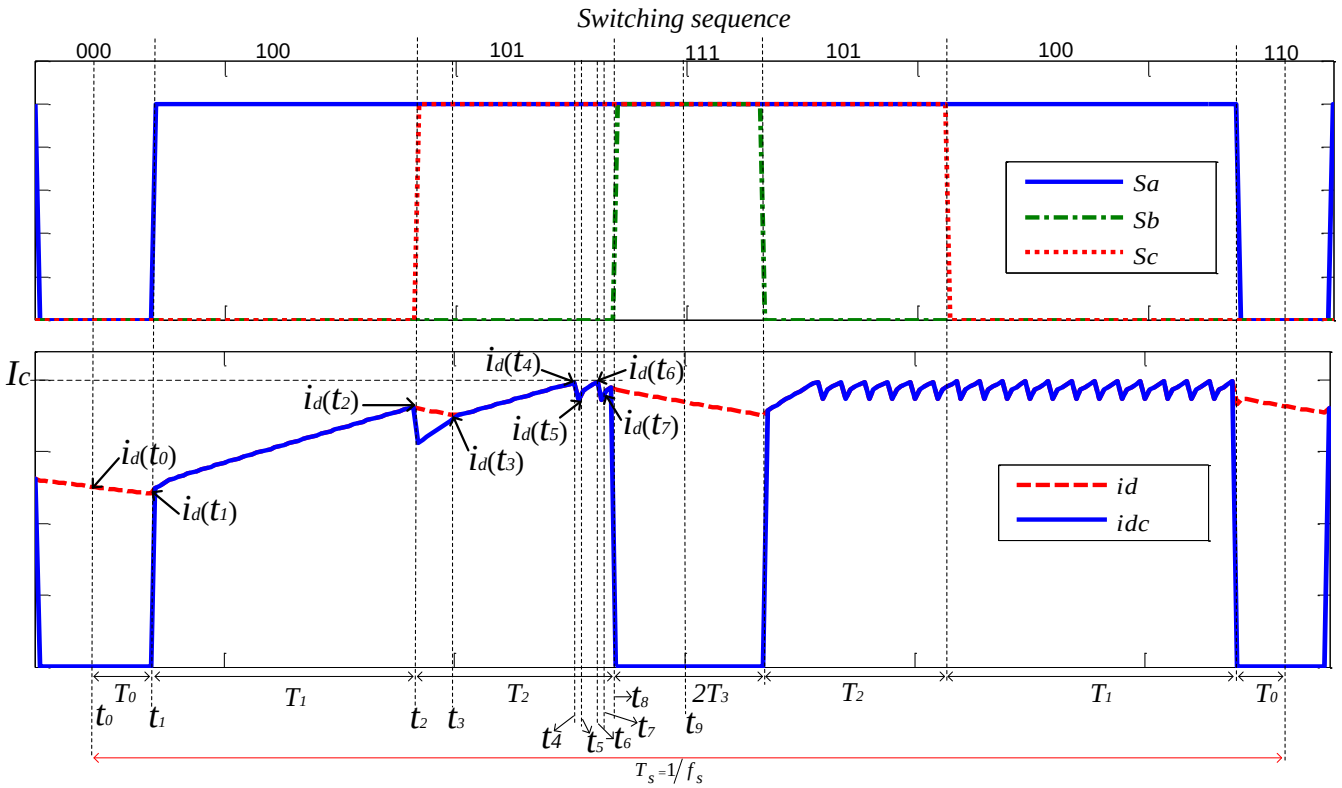

Fig. 3. SPWM output sequence from the VSI and measured DC link (i_{dc}) and DC inductor (i_d) currents during the fault condition.

$$i(t) = e^{-(t-t_1)/\tau_1}\left\{i_2 - \frac{V_{DC} - V_{ss} - 4V_d}{r_{c1}}\right\} + \frac{V_{DC} - V_{ss} - 4V_d}{r_{c1}} \tag{5}$$

where $L_e=L_s+L_f$, $r_e=r_s+r_f$, $\tau_1=3/2(L_e+L_d)/r_{c1}$, $r_{c1}=r_d+(3/2)r_e+(9/2)r_{on}$, $i_2=i_d(t_1)$, $i_a(t)=i_d(t)=i_{dc}(t)=i(t)$.

At $t=t_2$, the switching state changes to (101) and the DC inductor current instantaneously changes. According to Fig. 3, during t_2 to t_3, the DC inductor current is more than the DC link current and all of the diodes are ON. In this condition, the DC inductor is in discharging mode. Considering the equivalent circuit of Fig. 4(c), differential equation of (6) can be written for the DC inductor current.

$$\left(\frac{3}{2}L_e + L_d\right)\frac{di_b(t)}{dt} + \left(\frac{3}{2}r_e + \frac{5}{2}r_{on}\right)i_b(t) = V_{DC} - V_d \tag{6}$$

Equation (7) is derived by (6) and shows the DC link current formula in discharging mode.

$$i_b(t) = i_{dc}(t) = e^{-(t-t_2)/\tau_3}\left\{i_3 - \frac{V_{DC} - V_d}{r_{c2}}\right\} + \frac{V_{DC} - V_d}{r_{c2}} \tag{7}$$

where $i_3=i_d(t_2)$, $r_{c2}=(3/2)r_e+(5/2)r_{on}$, $\tau_3=((3/2)L_e+L_d)/(r_{c2})$.

In addition, the DC inductor current formula during discharging mode in this time interval can be expressed as:

$$i_d(t) = e^{-(t-t_2)(r_{d+}3r_{on})/L_d}\left\{i_3 + \frac{V_{ss}+2V_d}{r_d+3r_{on}}\right\} - \frac{V_{ss}+2V_d}{r_d+3r_{on}} \tag{8}$$

At $t=t_3$, the switching state is not changed but the DC link current reaches to the DC inductor current. So, the charging mode begins and continues until t_4 as shown in Fig. 3. Considering the equivalent circuit shown in Fig. 4(d), (9) can be expressed as follows:

$$(\frac{3}{2}L_e + L_d)\frac{di_d(t)}{dt} + (r_d + \frac{3}{2}r_e + \frac{9}{2}r_{on})i_b(t) = V_{DC} - V_{ss} - 3V_d \tag{9}$$

Solving (9) results in (10):

$$i_b(t) = i_d(t) = e^{-(t-t_3)/\tau_4}\left\{i_4 - \frac{V_{DC}-V_{ss}-3V_d}{r_{c3}}\right\} + \frac{V_{DC}-V_{ss}-3V_d}{r_{c3}} \tag{10}$$

where $i_4=i_d(t_3)=i_b(t_3)$, $\tau_4=(3/2L_e+L_d)/r_{c3}$ and $r_{c3}=(r_d+3/2r_e+9/2r_{on})$.

At $t=t_4$, the DC inductor current reaches to I_c. So, the control circuit turns off the SS. Now, the R is connected in series with the DC inductor. So from t_4, Mode 2 of operation starts.

Mode 2

During time interval of t_4 to t_5, the switching state is (101). According to Fig. 3, the DC link current equals to the DC inductor current. Considering the equivalent circuit of Fig. 4(e), (11) can be written for the DC inductor current.

$$(\frac{3}{2}L_e + L_d)\frac{di_b(t)}{dt} + (r_d + R + \frac{3}{2}r_e + \frac{7}{2}r_{on})i_b(t)) = V_{DC} - 3V_d \tag{11}$$

So we have:

$$i_d(t) = e^{-(t-t_4)/\tau_5}\left\{i_5 - \frac{V_{DC}-3V_d}{r_{c4}}\right\} + \frac{V_{DC}-3V_d}{r_{c4}} \tag{12}$$

where $i_d(t)=i_{dc}(t)$, $i_5=i_{dc}(t_4)=i_b(t_4)$, $\tau_5=(3/2L_e+L_d)/r_{c4}$, $r_{c4}=(r_d+R+3/2r_e+7/2r_{on})$.

It should be noted that the time interval of t_4 to t_5 is very small percentage of one switching period (T_s). At $t=t_5$, the control circuit turns on the SS. As a result, the R is bypassed. According to Fig. 3, from t_5 to t_6, the DC inductor current is equal with the DC link current and another charging mode begins and it continues until t_6. The equivalent circuit during time interval of t_5 to t_6 is shown in Fig. 4(f). At $t=t_6$, the control circuit turns off the SS. Therefore, the R is again connected in series with the DC inductor.

So from t_6 to t_7, the proposed approach will have the same operation of time interval of t_4 to t_5 (the corresponding equivalent circuit has been shown in Fig. 4(e)). At $t=t_7$, the SS turns on and bypasses the R. From t_7 to t_8, the proposed circuit operates as same as interval of t_5 to t_6 (the corresponding equivalent circuit has been shown in Fig. 4(f)).

It should be noted that, over the time interval of t_2 to t_8, the switching state is (101). At $t=t_8$, the switching state changes to (111). As shown in Fig. 3, at $t=t_8$, the DC link current instantaneously changes. In the meantime, as shown in Fig. 4(g), the DC inductor current begins to freewheel through the diodes D_1-D_3 and D_2-D_4. This situation will continue until $t=t_9$. After t_9, the circuit will have the operation condition as same as the time interval of t_4 to t_9 until the clearance of the fault. Fig. 4(h) and Fig. 4(i) show the DC inductor current after the fault removal. In this mode of operation, all of the diodes are ON and the DC inductor current decreases because of its resistance and forward voltage drop on the diodes and the SS. As these figures show, the DC inductor current quickly discharges to its pre-fault value that is equal with the peak value of the DC link current. In this way, the AR-FCL automatically becomes ready to limit any possible upcoming short circuit faults.

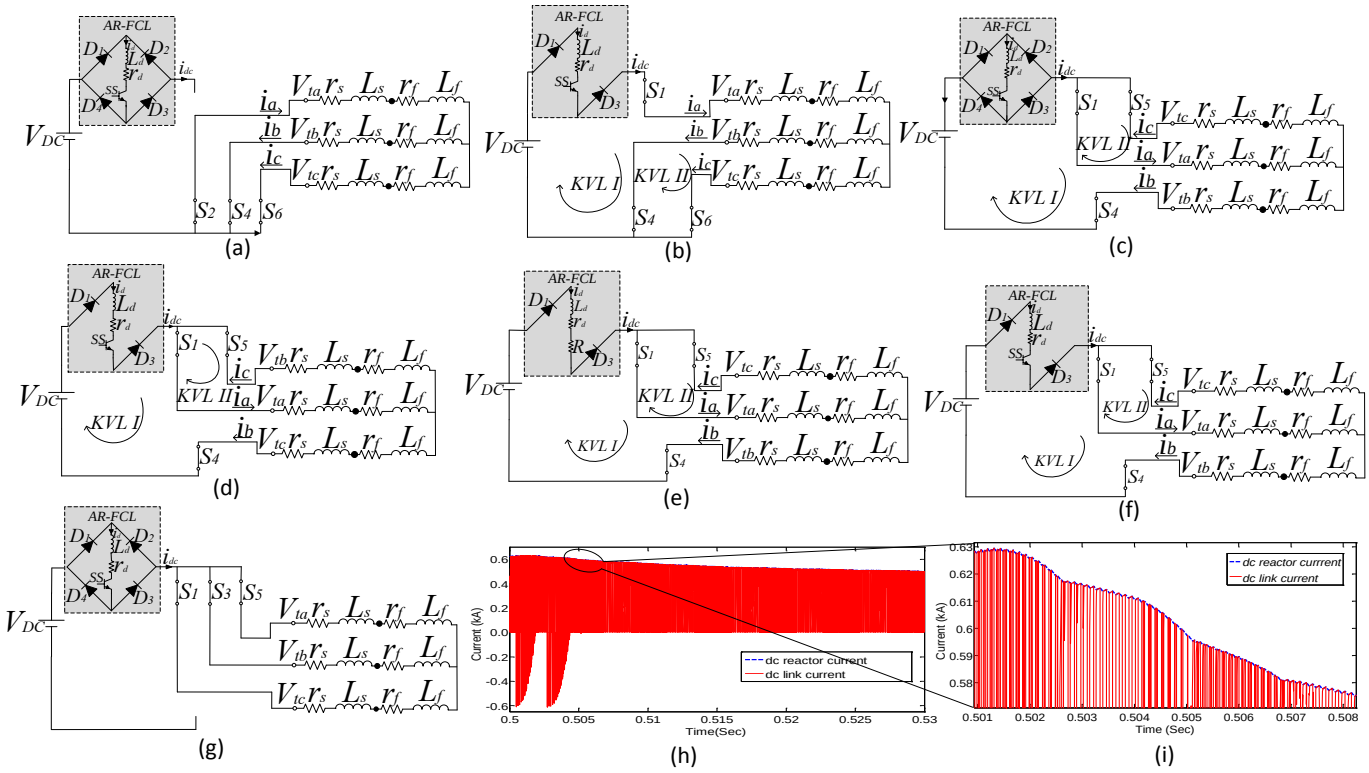

Fig. 4. Equivalent circuits of operating intervals during the fault condition. (a) Switching state:000 (b) Switching state:100 (c)-(f) switching state:101 (g) Switching state:111 (h)-(i) the DC inductor and the DC link current after the fault, (i) enlarged figure of (h).

V. Design Considerations

A. *Power Losses Calculation of the AR-FCL*

During one carrier period, the DC inductor current is a DC periodic current. Also, there are power losses and voltage drop across the DC inductor, the SS, and the diode-bridge. However, during the normal operation, due to the large value of the DC inductor, the DC inductor current is almost ripple-free with the amplitude of peak value of DC link current. So, (13) can be writing as follows:

$$I_r \cong 0 \Rightarrow I_{DC} \cong I_{\max} \tag{13}$$

where, I_r, I_{DC} and I_{max} stand for the ripple-current in the DC inductor, the average current in the DC inductor and the peak value of the DC link current in the steady state, respectively. So, the total power loss of the AR-FCL (P_{Total}) is sum of the DC inductor power loss (P_{DC}), power loss of the diode bridge (P_{Bridge}) power loss of the semiconductor switch (P_{ss}). Therefore, P_{Total} can be calculated as follows:

$$\begin{cases} P_{DC} \cong r_d I_{DC}^2 \\ P_{Bridge} + P_{SS} = 2V_d I_{DC} + V_{SS} I_{DC} \\ P_{Total} = P_{DC} + P_{Bridge} + P_{SS} = I_{DC}\left[r_d I_{DC} + 2V_d + V_{SS} \right] \end{cases} \tag{14}$$

On the other hand, without the AR-FCL and neglecting the switching power losses of the VSI, AC side and DC side active power of the VSI can be expressed as (15) [38].

$$\begin{cases} P_{ac\_inverter} = v_a i_a + v_b i_b + v_c i_c \\ P_{DC\_inverter} = V_{DC} i_P \\ P_{ac\_inverter} = P_{DC\_inverter} \end{cases} \tag{15}$$

Now, with the AR-FCL, the AC side active power of the VSI can be written as follows:

$$P_{ac\_inverter} = P_{DC\_inverter} - P_{Total} \tag{16}$$

The ratio of total power loss to the active power generated by the VSI is defined by K as follows:

$$K = \frac{P_{Total}}{P_{ac\_inverter}} = \frac{I_{DC}\left[r_d I_{DC} + V_{SS} + 2V_d \right]}{P_{ac\_inverter}} \tag{17}$$

For example, a VSI is considered with the rated capacity of 6 *MW*, output phase voltage of V_{abc_rms}=4 *kV*, *P.F*=0.9 and DC-link current of i_{p_rms}=600 *A*. By installation of the AR-FCL in series with DC link with the parameters of r_d=*0.01* Ω, V_{ss}=V_d=3 *V*, the P_{Total} is 9 *kW*. As a result, the *K* is 0.0015. The small value of *K* proves that in the presence of AR-FCL, the total power dissipation is very small percentage of overall rated power of the VSI and it can be ignored for most of practical applications.

B. Performance Evaluations

The issues, which should be taken into account as design considerations of the AR-FCL, are the DC inductor value, the value of *R*, the value of I_c, the impact of the fault impedance on the operation of the AR-FCL, and specifications of the SS of the AR-FCL.

B-1. Inductor size:

As mentioned, the L_{dc} is placed in series with the SS to protect it against severe *di/dt* at the beginning of fault occurrence. So, its value can be chosen considering current characteristics of the SS. Considering Fig. 3, the charging mode begins at t_1 after the fault occurs. As the worse condition, it is assumed that the fault happens exactly at the first moment of charging mode, t_1. Therefore, it is expected for especial value of the inductor, the maximum initial rate of current change will occur. By charging the inductor, its slop decreases, exponentially. So, by using (5), the initial rate of current change can be achieved as follows:

$$\frac{di_{dc}}{dt}=\frac{di_{a}}{dt}=\left[I_{peak}-\frac{V_{DC}-V_{SS}-4V_{d}}{r_{c1}}\right]\left[-\frac{r_{c1}}{L_{d}+\frac{3}{2}L_{e}}\right] \tag{18}$$

where I_{peak} is peak of the DC inductor current in the normal operation. Consequently, the minimum value of the inductor is expressed as follows:

$$L_{d}>\frac{V_{DC}-V_{ss}-4V_{d}-I_{Peak}r_{c1}}{di_{\max}/dt}-\frac{3}{2}L_{e} \tag{19}$$

di_{max}/dt is maximum permissible rate of the current change in the SS of the AR-FCL. However, the other fact should be taken into account is related to the inherent resistance of the DC inductor. It is completely obvious for large non-superconducting DC inductor; its inherent resistance will be large. As a result, considering the power loss in the DC inductor and di_{max}/dt of the SS, the DC inductor value can be calculated.

B-2. Resistance value:

In technical issues, the other parameter should be considered is the value of *R*. In order to control the magnitude of the i_d, in the proposed method, the *R* is used in parallel with the SS. As mentioned in section III, by operation of the SS, the *R* enters in series with the DC inductor. In this situation, regarding the maximum permissible current value (I_c), the *R* should be able to absorb the DC inductor energy to keep its current lower than the I_c. As a result, the rate of current change must be negative. Considering (12), at the first moment of Mode 2, t_4, when the DC inductor current reaches to I_c, the rate of current change is equal with (20).

$$\frac{di_{dc}}{dt}=\left[I_{c}-\frac{V_{DC}-3V_{d}}{r_{c4}}\right]\left[-\frac{1}{\tau_{5}}\right]e^{-(t-t_4)/\tau_{5}} \tag{20}$$

To achieve negative value for the rate of current change, the first part of (20) should be positive. In this case, the R is able to absorb the DC inductor energy and hold its current in I_c. As a result:

$$R > \frac{V_{DC} - 3V_d}{I_c} - r_d - \frac{3}{2}r_e - \frac{7}{2}r_{on} \tag{21}$$

Meanwhile, from switching point of view after the AR-FCL operation at t_4, considering Fig. 3, the DC inductor current decreases up to $I_c - \Delta I$. At t_5, the SS turns on and the DC inductor current charges until it reaches to I_c. As a result, this interval can be considered as one switching period of the SS of the AR-FCL ($T_{ss} = 1/f_{ss}$). So by using (12), the value of ΔI can be concluded as follows:

$$\Delta I \cong \left[I_c - \frac{V_{DC} - 3V_d}{r_{c4}} \right] \left[1 - e^{-(T_{ss}/2)/\tau_5} \right] \tag{22}$$

Therefore:

$$f_{ss} = \frac{1}{2\tau_5 \ln \left[\dfrac{I_c - \dfrac{V_{DC} - 3V_d}{r_{c4}}}{I_c - \dfrac{V_{DC} - 3V_d}{r_{c4}} - \Delta I} \right]} \tag{23}$$

f_{ss} depends on the R and mostly ΔI. Lower value of ΔI increases f_{ss}.

B-3. The value of I_c:

According to the analysis carried out in section IV, during the normal operation, the i_d equals to peak of the DC link current and it is employed to control the ON/OFF states of the SS. Therefore, in the present method, the current characteristics of the SDs of the VSI and also the maximum permissible current of the power system equipment must be considered to determine the I_c for the operation of the SS. So the value of I_c should be selected in a way that during the fault condition, the fault current through the SDs of VSI and also the AC side currents are restrained to their safe area operation.

B-4. The impact of the fault impedance:

From the fault impedance point of view, the performance of the proposed method during the three phase short circuit fault with the fault impedance $Z_f = r_f + jL_f\omega$ has been analysed in section IV. Considering the equations, which have been obtained in section IV, it is observed that the variation of r_f and L_f changes the time constant and magnitude of the steady state fault current component during the charging modes. In general, according to (10) and (12), increasing the Z_f is similar to the situation in which the impedance of the AR-FCL increases.

B-5. Specifications of semiconductor switch of the AR-FCL

According to (1), the DC link current is function of AC side currents that its amplitude is changed by switching states of the inverter semiconductors. Meanwhile, the equivalent circuits presented in Fig. 4(a) to Fig. 4(g) demonstrate the operational conditions with regard to (1). As Fig. 4 reveals during one switching carrier period, in some switching states, the DC link current equals to one of the inverter switches. In Fig. 4(b), the DC link current equals to i_a and from Fig. 4(c) to Fig. 4(f), the DC link current is equal with i_b. It means that from current rating point of view, the peak of current in both the SS located in the DC side and the inverter switches is same. However, if required to use series or parallel connections of the semiconductor switches both in the inverter or in the DC side switch, the state of art technologies guarantee the reliability of the system during the switching conditions [39]-[40].

VI. Simulation Results

Single line diagram of the test system is shown in Fig. 5. As shown in Fig. 5, the primary source is interconnected to the utility grid through the two level VSI, step-up transformer (with the same power rating of corresponding the VSI) and a double-line transmission line. The utility grid is represented by a three phase AC voltage source with equivalent impedance of Z_g. PSCAD/EMTDC software is implemented to simulate various fault conditions. To demonstrate the effectiveness of the proposed FRT scheme, different fault conditions are carried out including LLLG, LLG and LG faults. Out of all the different grid codes, which are regulated by the various operators, "*E.ON*" grid code has severe FRT requirements [18]. According to "*E.ON*", when voltage at point of common coupling drops to zero for 0.15 *s*, the DG must not be disconnected from the grid. So, in the all simulations, the fault lasts 0.15 *s*. Furthermore, in the literature, the fault current magnitude of the VSI is considered between 1 *p.u* and 2 *p.u* [5], [14]-[15]. However, in the present paper, the maximum permissible current magnitude for the VSI is assumed to be 2 *p.u* [14]. Table I shows the parameters of the simulated power system.

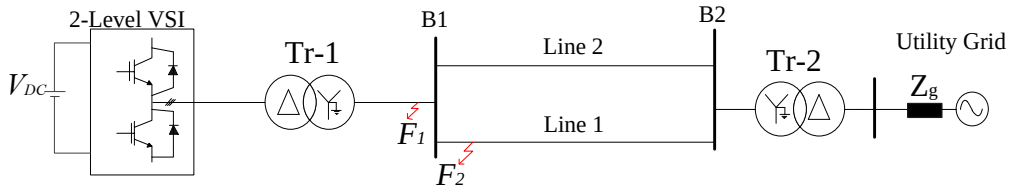

Fig. 5. The simulated power system.

A. *Symmetrical Faults*

In this scenario, a temporary LLLG fault is applied in point F1, as shown in Fig. 5, at t=0.8 s, for 0.15 s. This fault type, as a worst one, causes a sever voltage dip (100%) in the VSI terminal. At first, the simulation is carried out without the AR-FCL. The results are shown in Fig. 6(a) to Fig. 6(d). As shown in Fig. 6(a), once the fault occurs, the voltage at the VSI terminal drops to

zero value. In this condition, the VSI output current abruptly increases. AS shown in Fig. 6(b), its peak value reaches to around 4 *p.u*. Because, the maximum permissible current of the semiconductor switches is approximately two times of the nominal current [7], these over-currents damage the VSI. As aforementioned, a 2-level VSI employs six power electronic switches for DC to AC power conversions. The current through A phase (switches S_1 and S_2 in Fig. 1) are shown in Fig. 6(c). As Fig. 6(c) shows, these over-currents reach to about four times of the nominal value and tend to damage the semiconductor switches or trip out the VSI in the practical cases. Also, the DC link current is shown in Fig. 6(d). It is clear that there are a high level current and large distortions during the fault.

Table I. The simulation parameters

Transformers	**Tr-1**	4 *kV*/34.5 *kV*, 8 *MVA*, X=0.025 *p.u.*
	Tr-2	34.5 *kV*/115 *kV*, 47 *MVA*, X=0.025 *p.u.*
The AR-FCL	L_d=0.1 *H*, r_d=0.01 Ω, *R*=20 Ω, V_{drops} on the diodes and the IGBT=3 *V*	
Parallel lines	30 *km*, R_{line+}=0.1153 Ω*/km*, R_{line0}=0.413 Ω*/km*, L_{line+}=1.05 *mH/km*, L_{line0}=3.32 *mH/km*, C_{line+}=11.33 *nF/km*, C_{line0}=5.01 *nF/km*	
Utility grid	115 *kV*, 2500 *MVA*, X/R=7	

To demonstrate the effectiveness of the proposed FRT approach, the temporary LLLG fault with the same fault characteristics of the previous study is occurred at point F1, in Fig. 5, whereas the AR-FCL is connected in series with the DC link of the VSI. Corresponding results are provided in Fig. 7(a) to Fig 8(d). The DC inductor current is shown in Fig. 7(a). It is clear that during the fault, the DC inductor current is effectively restricted to the pre-defined fault current level. Moreover, considering Fig. 7(b), the effective operation of the proposed AR-FCL limits the VSI three phase fault current to less than twice of the nominal current. Also, the currents through A phase SDs are shown in Fig. 7(c). It is obvious that during the voltage dip, A phase SDs currents are limited to the pre-defined current value. So, the SDs operate in the safe area during the fault condition. In addition, the DC link current is also presented in Fig. 7(d). Considering this figure, the DC link current has slightly smooth variation during the fault and is limited to the pre-defined value.

B. Asymmetrical Faults

As aforementioned, the performance of the proposed AR-FCL is assessed during all grid fault types. In this section, the effectiveness of the proposed FRT approach is investigated during the asymmetrical grid faults. For this purpose, two cases of asymmetrical fault including LLG fault (B and C phases to G), and LG fault (A phase to G) are applied at the point F1 in Fig. 5, at *t*=0.8 *s* for 0.15 *s*. For the LLG fault, three phase output currents, current through A phase SDs, the DC link current and the DC inductor current of the VSI are shown in Fig. 8(a) to Fig. 8(f). It is obvious that by applying the proposed AR-FCL not only the

currents have been limited but also the distortion on the DC link current has been restricted. It means that the VSI can operate in the safe and reliable area without any damage during LLG fault.

In Fig. 9, the performance of VSI is evaluated during LG fault. Like the other grid faults, utilising the proposed scheme causes effective limitation on the fault current and guarantees the operation of VSI.

The other fact, which should be considered about employing the AR-FCL, is about the limiting characteristic of the DC inductor during the first moments of the fault and before the operation of the SS. It is clear that the time interval between the fault initiation and the SS operation is very small [41] than required time for operating the protection devices and disconnecting the VSI from the utility grid. So, the severe *di*/*dt*, which is initiated during the initial instants of the fault, can damage the SDs of the VSI. The rate of change of current through one of the SDs of the VSI, at the first moment of fault, for both situations including with and without the proposed AR-FCL in the DC link of the VSI, is compared to each other in Fig. 10. According to Fig. 10, the AR-FCL can suppress the severe *di*/*dt* in the initial instants of fault occurrence in comparison with the case that any FRT measure is not included. According to this analysis, by implementation of the proposed FRT scheme, the VSI can stay connected to the utility during the worst case short circuit fault at the point F1. So, it complies with the new grid code requirements.

C. *Repeated Transient Faults*

Repeated transient faults are introduced as a major problem in the overhead lines. The intent of this section is to highlight the performance of the proposed FRT scheme in the repeated transient short circuit faults. For this purpose, at t=0.6 s, the LG fault (A phase to G) repeated transient short-circuit fault happens at the point F2 in Fig. 5. Corresponding results are provided in Fig. 11. It is obvious that after clearance of the first fault, the AR-FCL returns to its normal operation condition as soon as possible and it is ready to limit the next fault. In fact, the proposed AR-FCL can successfully limit the VSI fault current during such critical circumstances.

VII. Experimental Results

To prove the both analytical analysis and the simulation results of the proposed FRT approach, a three phase VSI including the proposed AR-FCL is tested. Fig. 12 shows experimental set-up configuration. In addition, parameters of the experiment are presented in Table II. The VSI is controlled through use of MATLAB and Dspace CP1104. To apply the different types of the fault, a TTL controlled contactor RS 324-053 is utilised. However, it should be noticed that to control the fault current level a fault impedance is also employed. This fault impedance is a variable resistor 0-18.5 Ω that has been adjusted in 10% during the fault. As it is well-known, there are always experimental errors, which are mostly related to the measurement devices. Therefore, firstly, these issues are considered. Due to huge amount of noises, which are generated by the SDs of the VSI, the current transformers (CTs), which are used to measure the AC output currents of the VSI and one of the SDs, have 1/5

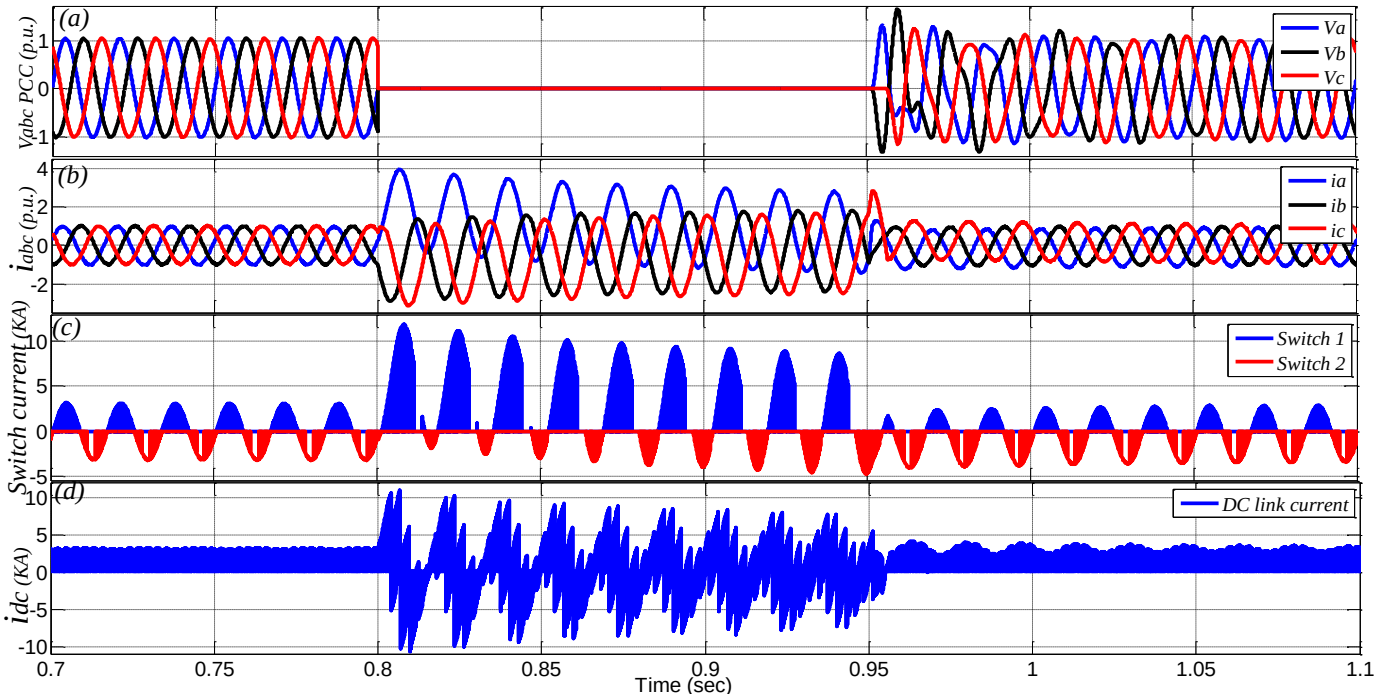

Fig. 6. Simulation results for the LLLG fault at point F1 without the proposed AR-FCL, (a) three-phase voltages at point F1, (b) three-phase output currents of the VSI, (c) A phase switch current of the inverter, (d) the DC link current.

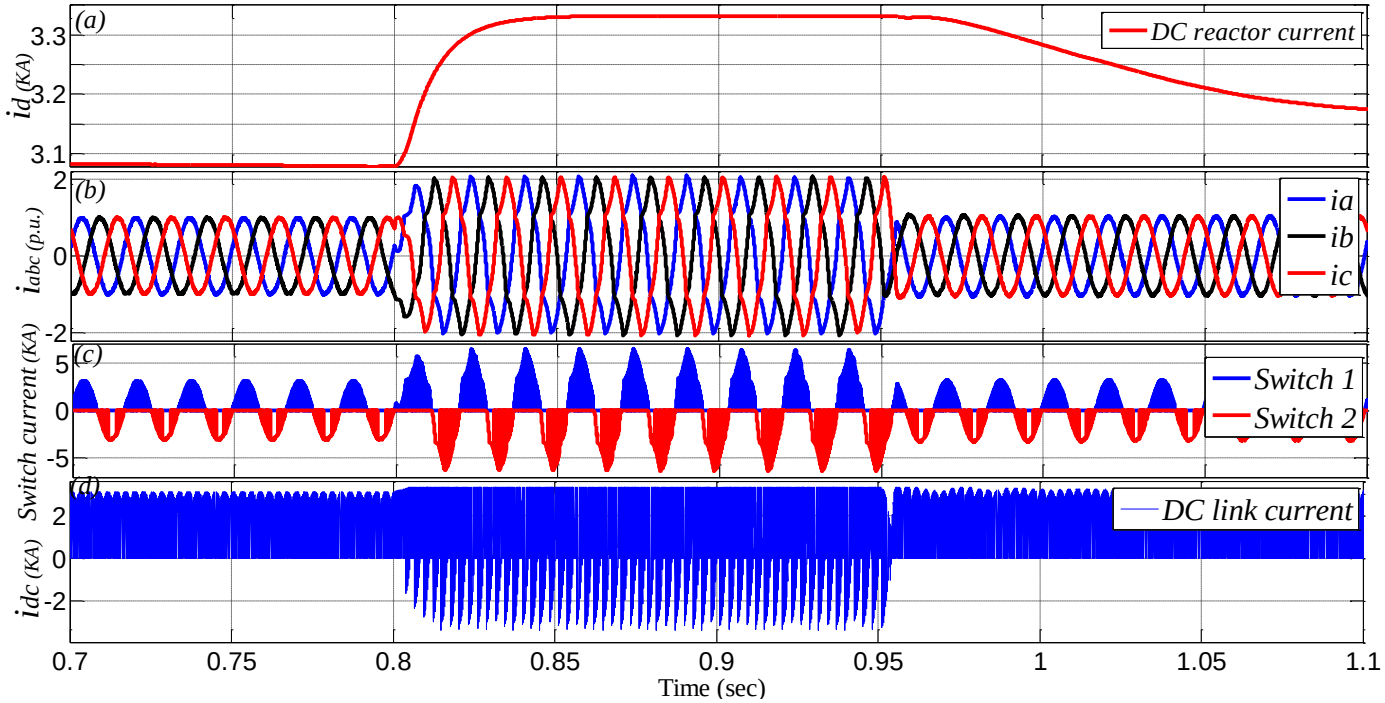

Fig. 7. Simulation results for the LLLG fault at point F1 when the proposed AR-FCL is employed, (a) the DC inductor current, (b) three-phase output currents of the VSI, (c) A phase switch current of the inverter, (d) DC link current.

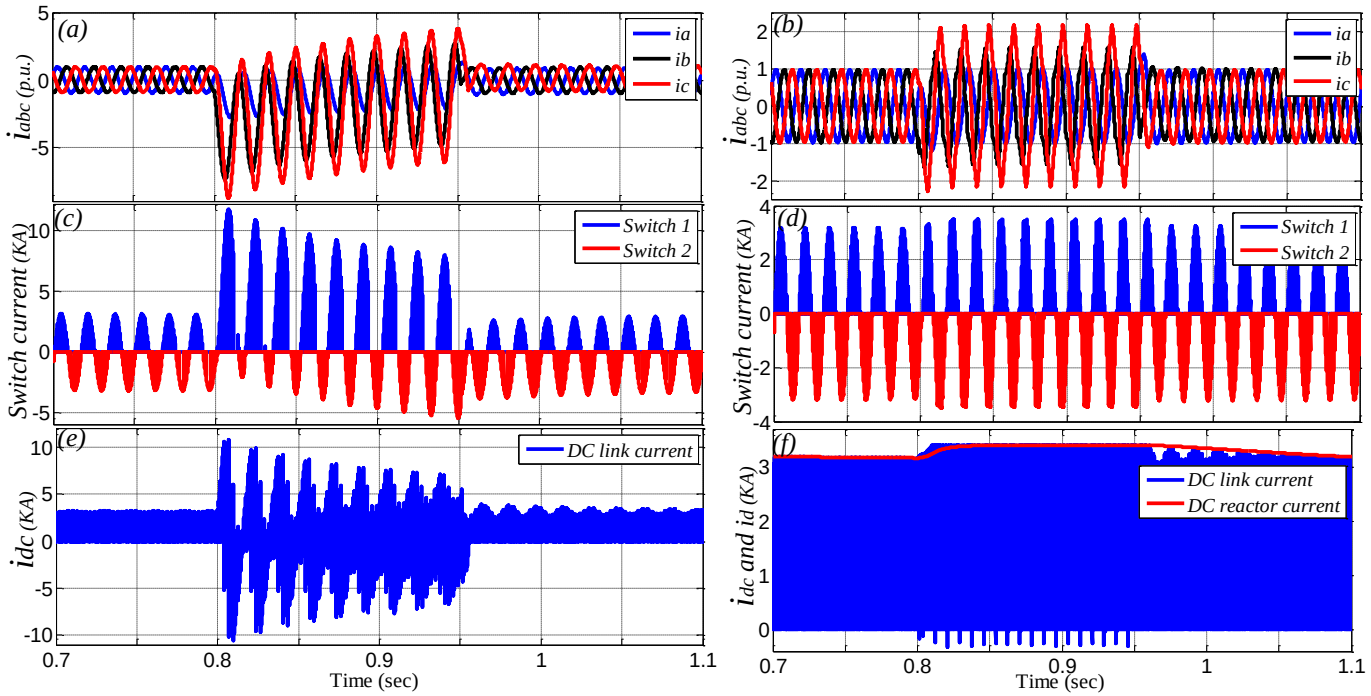

Fig. 8. Simulation results for an LLG fault at point F1. Three-phase output currents of VSI: (a) without the AR-FCL, (b) with the AR-FCL. A phase switches current of inverter: (c) without the AR-FCL, (d) with the AR-FCL. DC link current and DC inductor current: (e) without the AR-FCL, (f) with the AR-FCL.

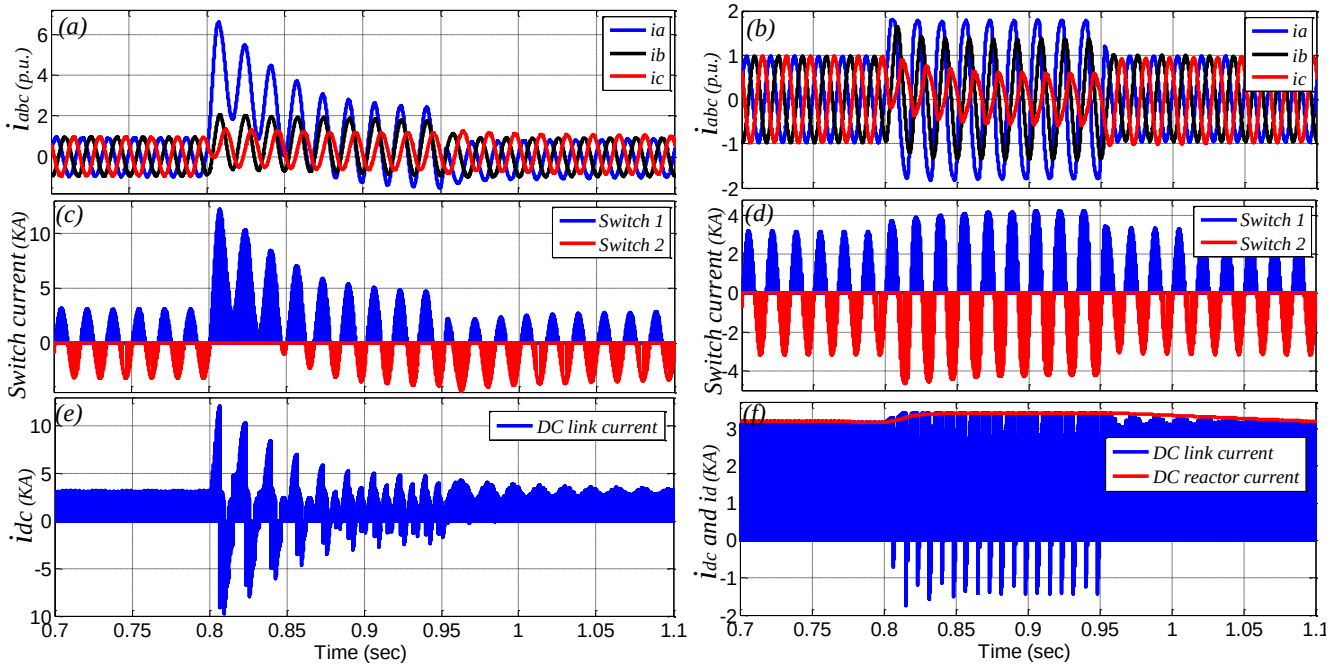

Fig. 9. Simulation results for an LG fault at point F1. Three-phase output currents of VSI: (a) without the AR-FCL, (b) with the AR-FCL. A phase switches current of inverter: (c) without the AR-FCL, (d) with the AR-FCL. DC link current and DC inductor current: (e) without the AR-FCL, (f) with the AR-FCL.

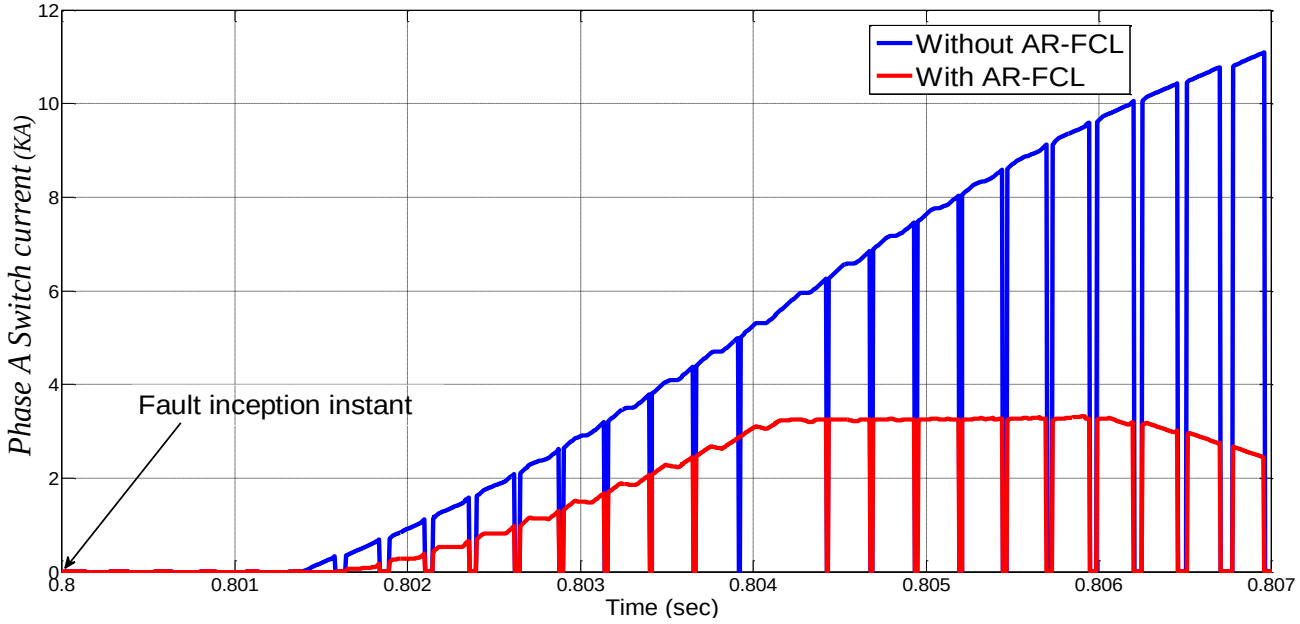

Fig. 10. Effectiveness of the proposed FRT scheme in suppressing the initial rate of current change in the SDs of the VSI.

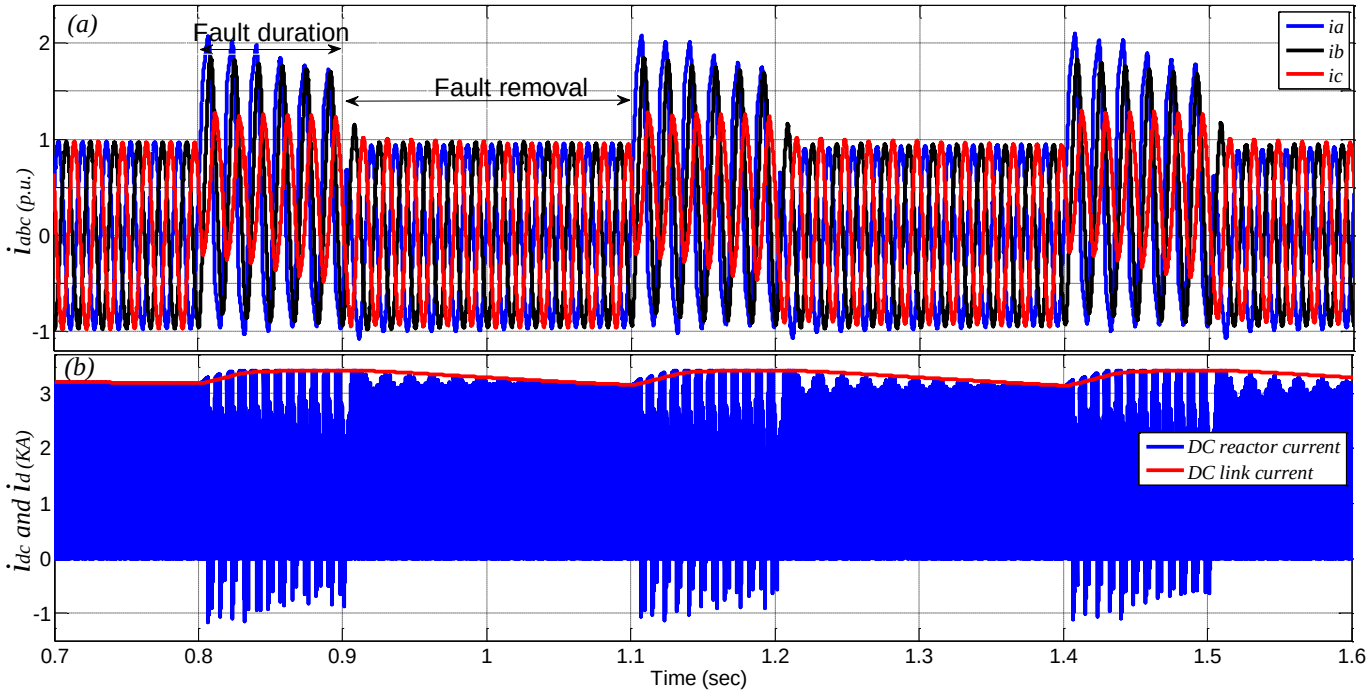

Fig. 11. Performance of the proposed FRT scheme during LG repeated transient fault at point F2. (a) three-phase output currents of VSI. (b) DC link current and DC inductor current.

ratio. This way helps to decrease the noises of the AC side, which affect captured figures by the oscilloscope. Therefore, Amperes per Division on the screen of the oscilloscope should be divided to 5. For the DC side currents including the DC link current and the DC inductor current, the Ampere per Division is the same, which is shown on the screen of the oscilloscope. Also, volt per division is 100 V per division. Time per division and the output frequency for all experimental figures are shown on the screen of oscilloscope. For all fault types except the transient faults, the fault duration is 0.15 *s*. During the transient faults, the fault interval

is considered 0.1 *s* and the time between two repeated transient faults is adjusted for 0.2 *s*.

A. Symmetrical Faults

First, LLLG fault is applied to the experimental circuit at point F in Fig. 12 without the proposed AR-FCL. To do this test, it is required to use an inverter without any self-protection. As a result, three modules of superfast NP-IGBT are utilised to make a three phase inverter. Corresponding results of LLLG fault are shown in Fig. 13 with and without the proposed scheme.

In Fig. 13(a), the line-to-line voltage of B and C phases decreases to near zero value during the fault. Fig. 13(f) shows that the fault currents are limited to 2 *A* by using the proposed AR-FCL. But without the proposed approach, the fault currents in both DC side and AC side increase up to 6 *A* (Fig. 13(b) and Fig. 13(d)). The other fact is about the DC inductor limiting characteristic. Comparing Fig. 13(c) and Fig. 13(g) proves that the raising edge of fault current in A phase SDs of the VSI decreases, significantly. Also, as aforementioned, considering Fig. 13(d) and Fig. 13(h), applying the AR-FCL smooths the DC link current during the fault.

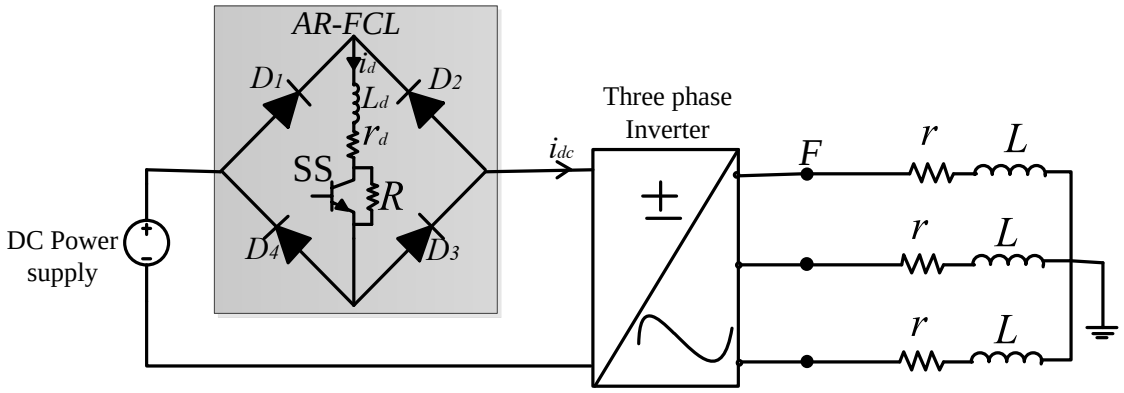

Fig. 12. Single line diagram of the experimental set-up.

Table II. The experiment parameters

DC power supply	Two series GPC-3030, V_{rated}=120 *V*, I_{rated}=3 *A*, V_{dc}=80 *V*
The AR-FCL	L_d=0.1*H*, r_d=0.5 Ω, R=35 Ω
	The SS: IGBT, Type: IKW75N60T, 600 *V*, 75 A, VCE(sat)=1.5 *V*
	The single phase diode rectifier bridge: BR354, 400 *V*, 35 *A*, V_F=1.1 *V*
Three phase inverter	VCS, SPWM, Carrier frequency: 1080 *Hz*, output frequency=60 *Hz*, The SDs: Superfast NPT-IGBT modules, SKM50GB063D, 600 *V*, 50 *A*, VCE(sat)=2.1 *V*
The load	Variac Transformer: 50B G3M, 0-465 *V*, 2.5 *A*

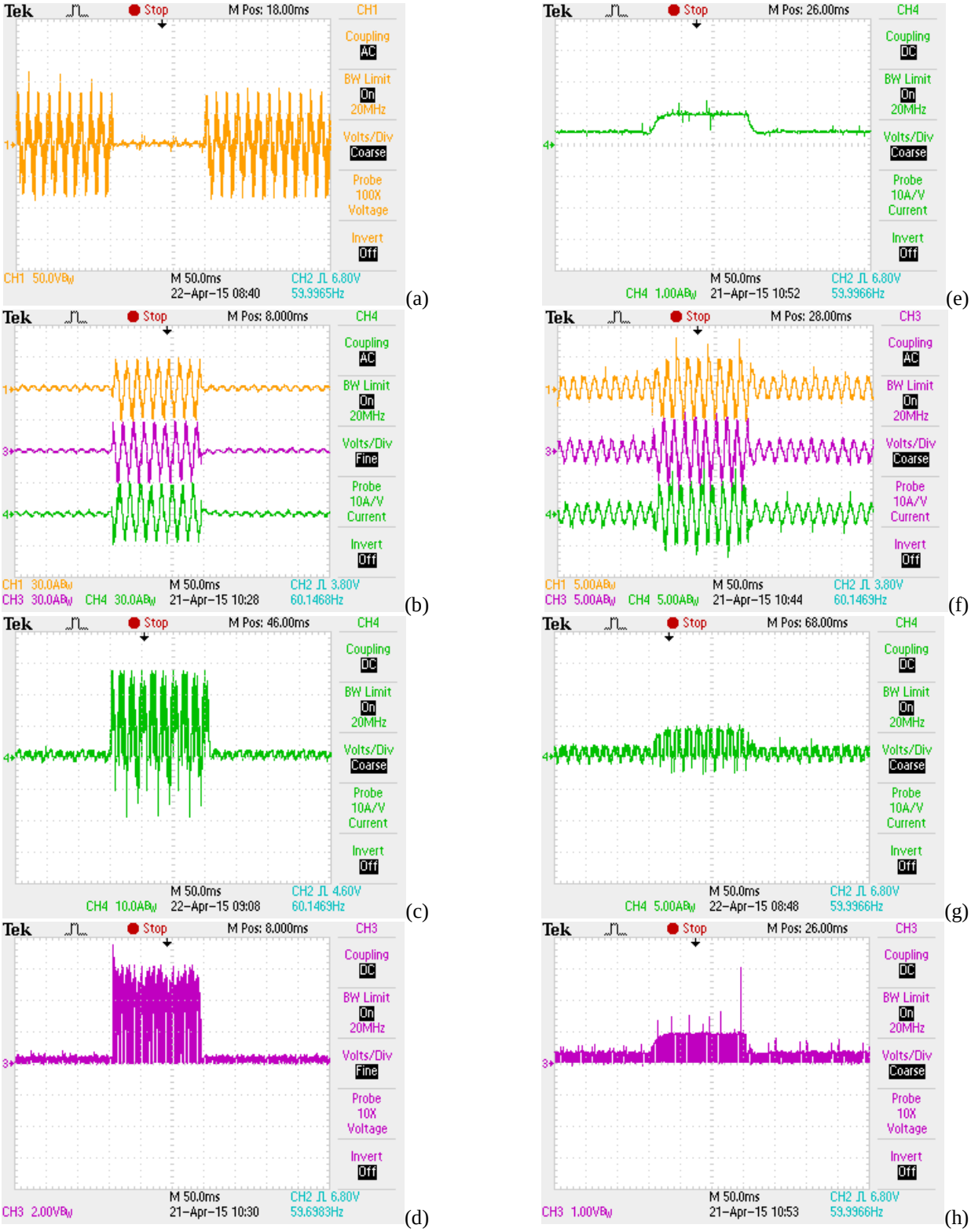

Fig. 13. Experimental results during LLLG fault. (a) Line to line voltage, B and C phases. Without the AR-FCL: (b) AC output currents of the VSI, (c) the SD A phase current of the VSI, (d) DC link current. With the AR-FCL: (e) the DC inductor current, (f) AC output currents of the VSI, (g) the SD A phase current of the VSI, (h) DC link current.

B. Asymmetrical Faults

This section deals with LLG and LG faults. The results for LLG and LG are shown in Fig. 14 and Fig. 15, respectively. As expected, by employing the AR-FCL, the AC output currents of the VSI and also the DC link current are restrained. Fig. 16 shows how the DC inductor can make a safe condition for the SDs of the VSI in the initial instants of fault occurrence. In fact, the AR-FCL not only restrains the fault current level, but also the severe *di*/*dt* decreases in a good manner.

C. Repeated Transient Faults

In this section, two repeated LG transient faults are applied to the experimental set-up. As aforementioned, the fault duration is 0.1 *s* and the time interval between the faults is 0.2 *s*. Considering Fig. 17, it is obvious that not only the AC output currents in the first fault is limited but also the DC inductor discharges quickly and the AR-FCL becomes ready to operate for the next fault.

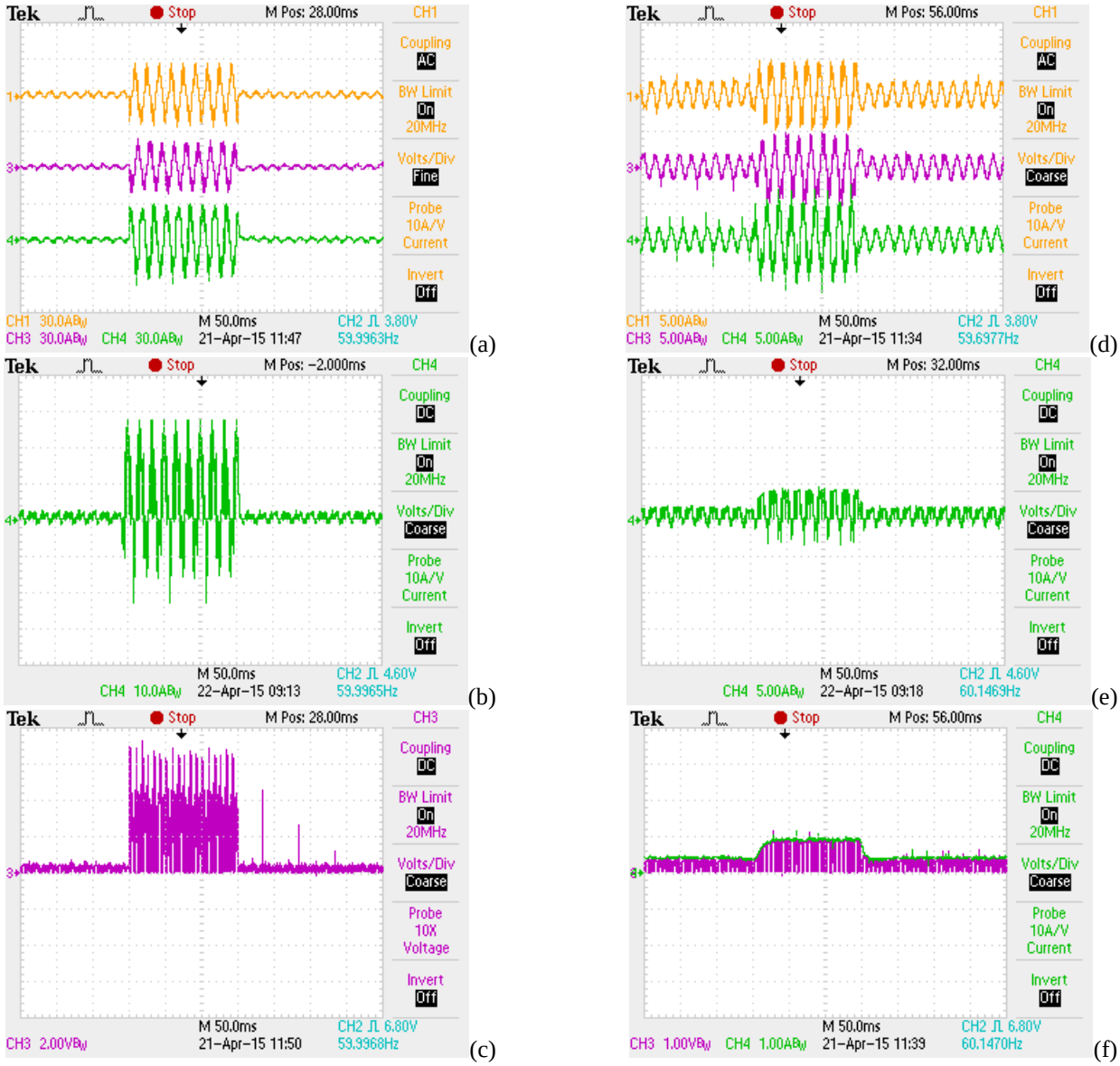

Fig. 14. Experimental results during LLG fault. Without the AR-FCL: (a) AC output currents of the VSI, (b) the SD A phase current of the VSI, (c) DC link current. With the AR-FCL, (d) AC output currents of the VSI, (e) the SD A phase current of the VSI, (f) DC link current and DC inductor current.

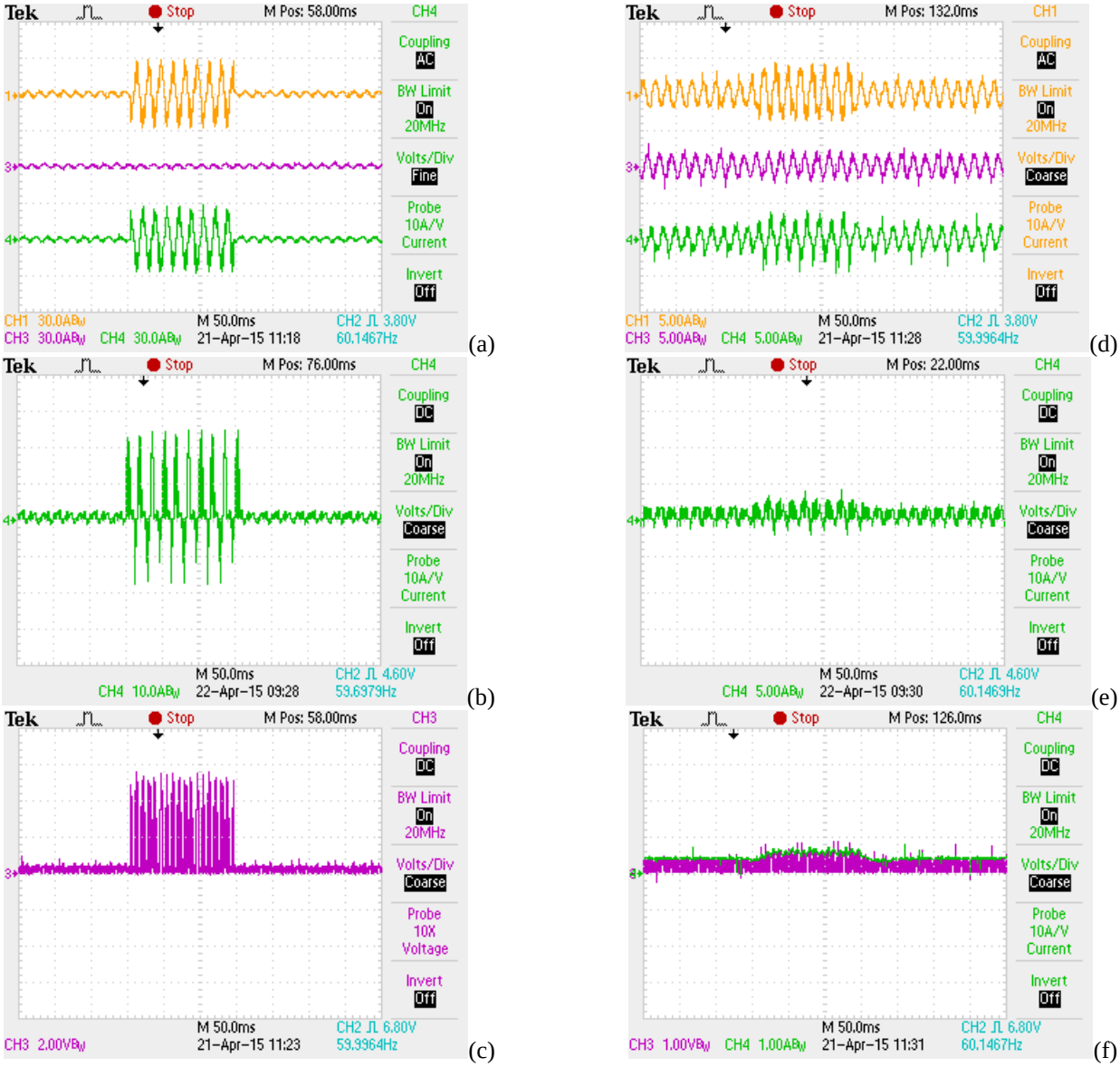

Fig. 15. Experimental results during LG fault. Without the AR-FCL: (a) AC output currents of the VSI, (b) the SD A phase current of the VSI, (c) DC link current. With the AR-FCL: (d) AC output currents of the VSI, (e) the SD A phase current of the VSI, (f) DC link current and DC inductor current.

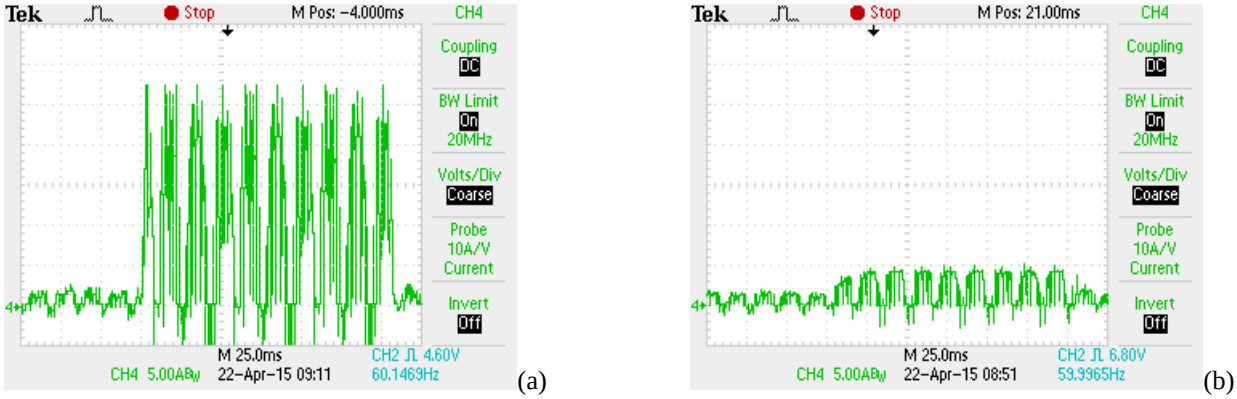

Fig. 16. Experimental results about limiting the severe *di*/*dt* of the current in the initial moments of the fault in the SDs of the VSI (a) without the AR-FCL (b) with the AR-FCL.

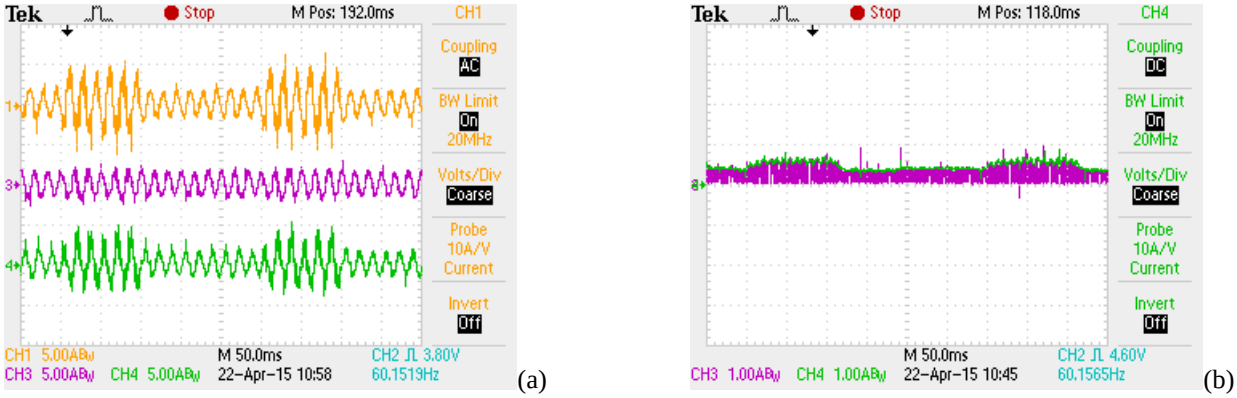

Fig. 17. Experimental results during LG repeated transient faults at point F with the proposed FRT scheme. (a) three-phase output currents of the VSI. (b) DC link current and DC inductor current of the VSI.

VIII. Conclusion

This paper presented the novel DC link AR-FCL based FRT scheme to improve the FRT capability in the VSI. The proposed approach only uses one set of single phase AR-FCL, which is placed in the DC side of the VSI. Therefore, this approach reduces the number of the required FCLs, which are used in the AC side of the VSI. In addition, in the proposed AR-FCL due to implementing the non-superconducting DC inductor, the initial cost also decreases. The VSC strategy is employed during the normal operation as well as during the fault condition with the AR-FCL. This characteristic is interesting for the industry, because in the other FRT methods, the control strategy of VSI is changed from the VSC to the CSC during the fault to restrict the fault current level. The proposed AR-FCL can suppress severe *di/dt* at the first moments of the fault and protect the SDs of the VSI from damage even at zero grid voltage, as recommended by new grid codes, with a high degree of reliability. Experimental and simulation studies have been carried out and there are good agreements between the results. It is clear that the proposed approach has reliable performance during both symmetrical and asymmetrical faults. To sum up, the proposed method can be easily implemented by commercial inverter manufacture companies with the least technical design of the inverter from the practical point of view.

IX. Acknowledgment

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